CLAIMS

1. A semiconductor device comprising:

a substrate including a plurality of holes and a surface over which an interconnecting pattern is formed, part of the interconnecting pattern being superposed over the holes;

a semiconductor chip disposed over another surface of the substrate and including a plurality of electrodes to be positioned over the holes; and

conductive members provided within the holes for electrically connecting the electrodes to the interconnecting pattern.

2. The semiconductor device as defined in claim 1,

wherein a resin is provided between the substrate and the semiconductor chip.

3. The semiconductor device as defined in claim 2,

wherein the resin is an anisotropic conductive material containing conductive particles; and

wherein the conductive members are electrically connected to the interconnecting pattern through the conductive particles.

4. The semiconductor device as defined in claim 1,

wherein part of the interconnecting pattern closes the holes.

5. The semiconductor device as defined in claim 1,

wherein the interconnecting pattern includes a plurality of interconnecting lines; and

wherein two or more interconnecting lines extend over each of the holes.

6. The semiconductor device as defined in claim 1,

wherein the other surface of the substrate is roughed.

7. The semiconductor device as defined in any one of claims 1 to 6,

wherein a recognition hole is formed in the substrate at a position differing from the holes; and

wherein a recognition pattern is formed over the recognition hole on the side of a surface of the substrate including the interconnecting pattern.

8. The semiconductor device as defined in claim 7,

wherein the recognition hole is formed in the substrate outside a mounting region for the semiconductor chip.

9. The semiconductor device as defined in claim 7,

wherein the recognition pattern includes:

a first pattern extending in the X-axis direction of the two-dimensional coordinate system established on a surface of the substrate; and

a second pattern extending in the Y-axis direction.

10. The semiconductor device as defined in any one of claims 1 to 6,

wherein the conductive members are a plurality of layered bumps.

11. The semiconductor device as defined in claim 10,

wherein the bumps include first bumps formed on the electrodes and second bumps formed on the first bumps.

12. The semiconductor device as defined in claim 11,

wherein at least the first bumps are ball bumps.

13. The semiconductor device as defined in claim 11,

wherein the second bumps are formed of a metal which has a melting point lower than the melting point of the first bumps.

14. The semiconductor device as defined in claim 13,

wherein the first bumps are formed of gold.

15. The semiconductor device as defined in claim 14,

wherein the second bumps are formed of solder.

16. The semiconductor device as defined in claim 11,

wherein the first bumps and the second bumps are formed of the same material.

17. The semiconductor device as defined in any one of claims 1 to 6,

wherein the semiconductor chip is mounted face-down to the substrate.

18. A circuit board over which is mounted the semiconductor device as defined in any one of claims 1 to 6.

19. An electronic instrument provided with the semiconductor device as defined in any one of claims 1 to 6.

20. A method of fabricating a semiconductor device comprising the steps of:

preparing a substrate including a plurality of holes and an interconnecting pattern which extends partially over the holes, and also preparing a semiconductor chip having a plurality of electrodes which have conductive members formed on the electrodes; and

disposing the conductive members within the holes and mounting the semiconductor chip over the substrate to connect electrically the interconnecting pattern to the electrodes through the conductive members.

21. The method of fabricating a semiconductor device as defined in claim 20, further comprising

a step of providing a resin over the substrate in a region

for mounting the semiconductor chip.

22. The method of fabricating a semiconductor device as defined in claim 21,

wherein the resin is an anisotropic conductive material containing conductive particles; and

wherein after the provision of the resin, the conductive members are electrically connected to the interconnecting pattern through the conductive particles.

23. The method of fabricating a semiconductor device as defined in claim 20,

wherein the holes are formed in the substrate to be positioned under the electrodes;

wherein part of the interconnecting pattern closes the holes; and

wherein the conductive members is disposed within the holes.

24. The method of fabricating a semiconductor device as defined in claim 21,

wherein the interconnecting pattern includes a plurality of interconnecting lines;

wherein two or more of the interconnecting lines extend over each of the holes in the substrate; and

wherein two or more of the conductive members are disposed within each of the holes.

25. The method of fabricating a semiconductor device as defined in claim 24,

wherein the step of providing a resin includes a step of mounting the substrate over a member;

wherein the member has properties which repel the resin at least in a region facing the holes in the substrate; and

wherein the resin is provided after the mounting of the substrate over the member with a surface of the substrate having the interconnecting pattern to face the member.

26. The method of fabricating a semiconductor device as defined in claim 20, further comprising

a step of roughing the other surface of the substrate.

27. The method of fabricating a semiconductor device as defined in any one of claims 20 to 26, further comprising

a step of forming a recognition hole in the substrate at a position differing from the holes, and forming a recognition pattern over the recognition hole on the side of a surface of the substrate including the interconnecting pattern.

28. The method of fabricating a semiconductor device as defined in claim 27,

wherein the recognition pattern includes:

a first pattern extending in the X-axis direction of the two-dimensional coordinate system established on a surface of

the substrate; and

a second pattern extending in the Y-axis direction; and

wherein positioning of the semiconductor chip and the substrate is carried out by using the recognition pattern.

29. The method of fabricating a semiconductor device as defined in any one of claims 20 to 26,

wherein the conductive members are a plurality of layered bumps.

30. The method of fabricating a semiconductor device as defined in claim 29,

wherein the bumps are formed by:

a first step of bonding a first conductive wire to one of the electrodes of the semiconductor chip and cutting the bonded first conductive wire with part of the first conductive wire to remain on one of the electrodes;

a second step of forming a first bump by pressing the remaining part of the first conductive wire on the electrode;

a third step of bonding a second conductive wire to the first bump and cutting the bonded second conductive wire with part of the second conductive wire to remain on the first bump; and

a fourth step of forming a second bump by pressing the remaining part of the second conductive wire on the first bump.

31. The method of fabricating a semiconductor device as

defined in claim 30,

wherein the first step is repeated for the plurality of electrodes to provide each of the electrodes with part of the first conductive wire; and

wherein the remaining parts of the first conductive wires on the electrodes are simultaneously pressed to form the first bumps at a time in the second step.

32. The method of fabricating a semiconductor device as defined in claim 31,

wherein the third step is repeated to provide each of the first bumps with part of the second conductive wire; and

wherein the remaining parts of the second conductive wires on the electrodes are simultaneously pressed to form the second bumps at a time in the fourth step.

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